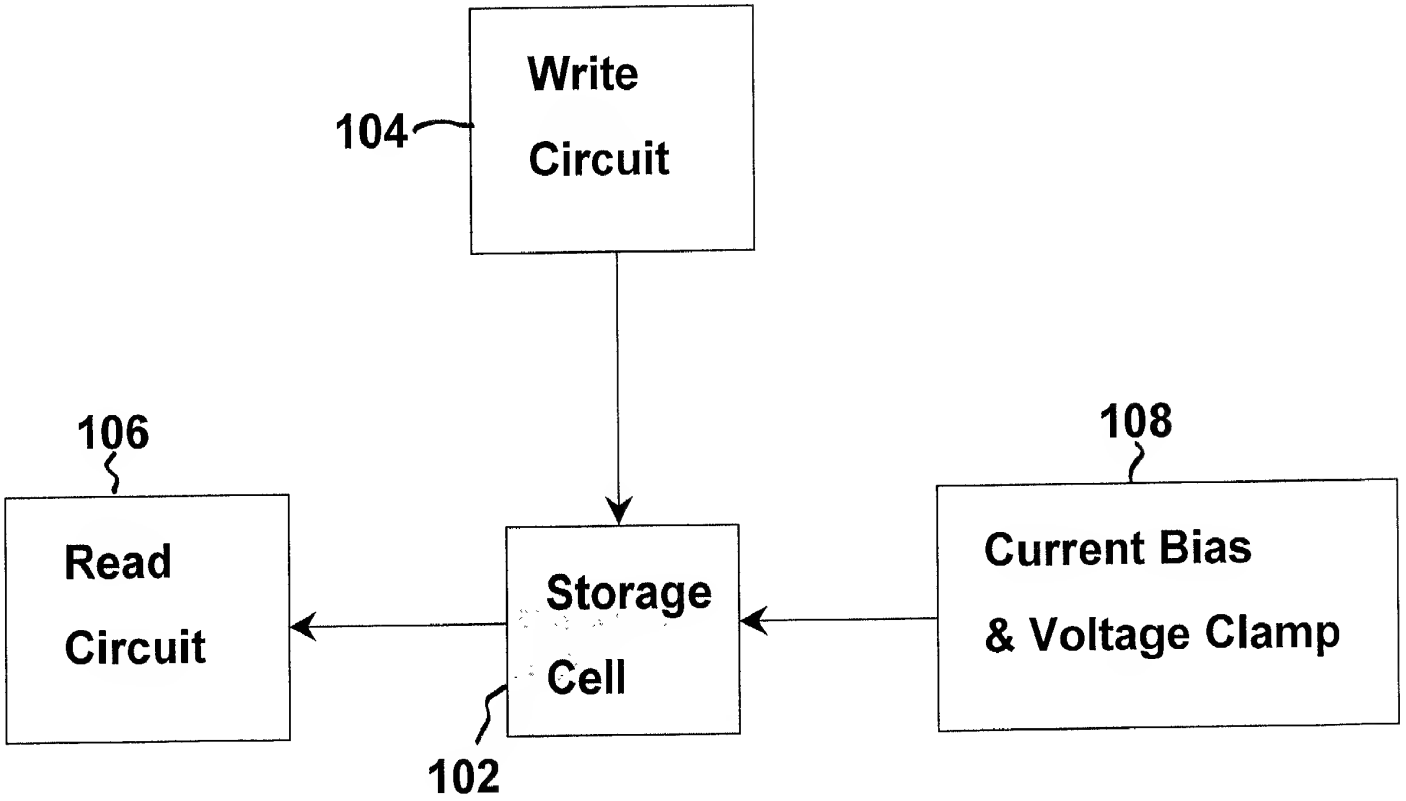
Write
Circuit
104
106
Read
Circuit
Storage
Cell
102
108
Current Bias
& Voltage Clamp

FIG. 1

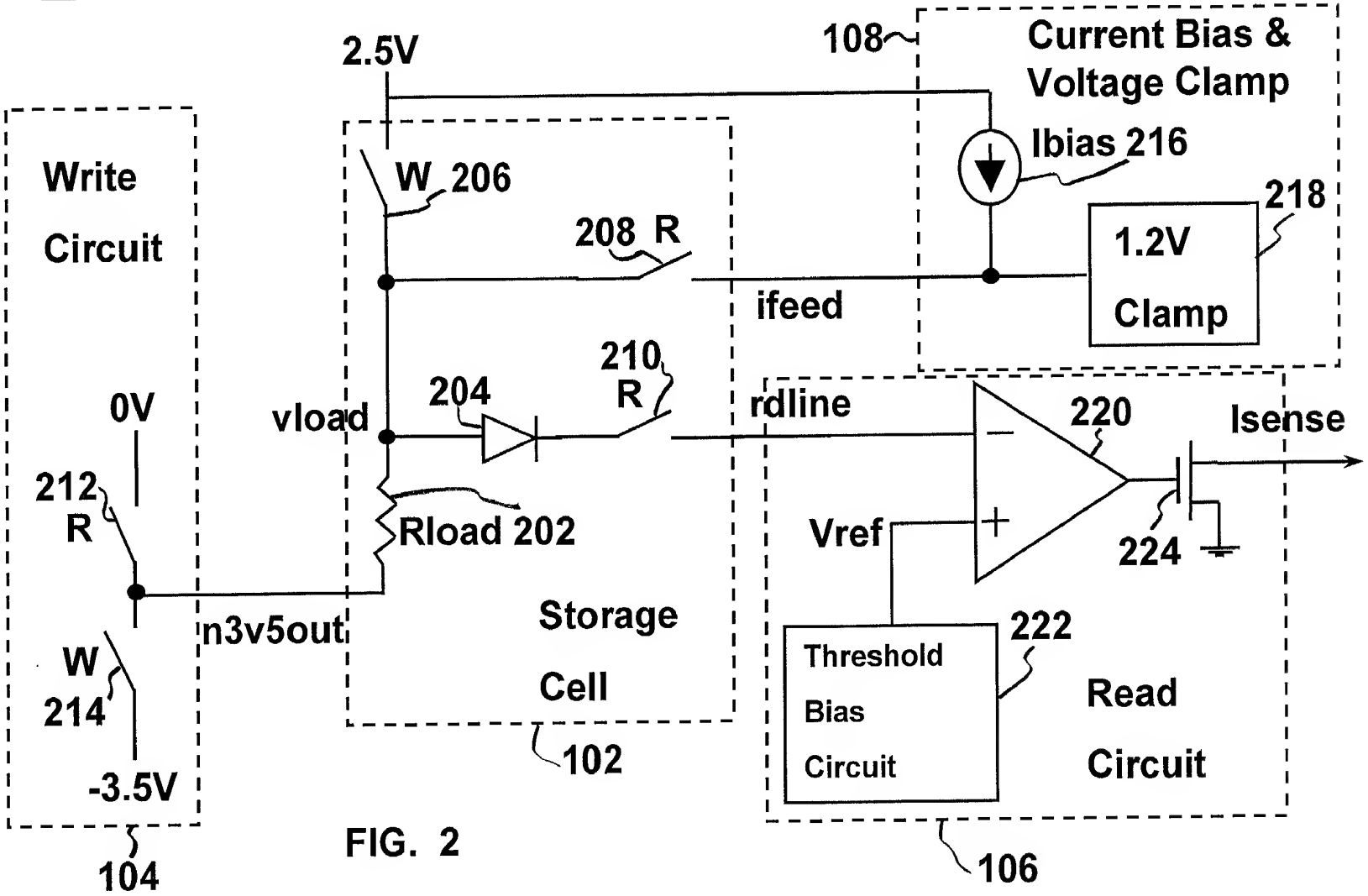

FIG. 2

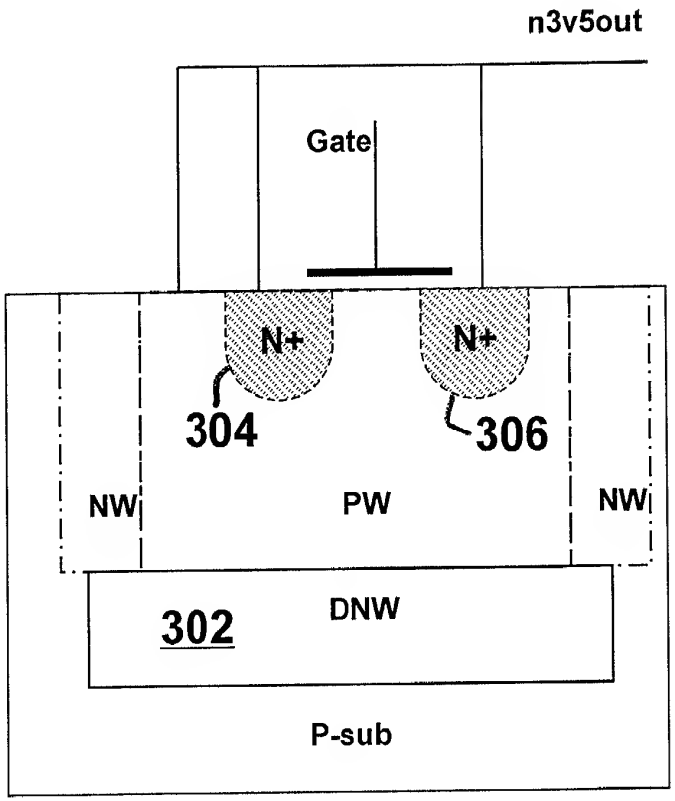

FIG. 3

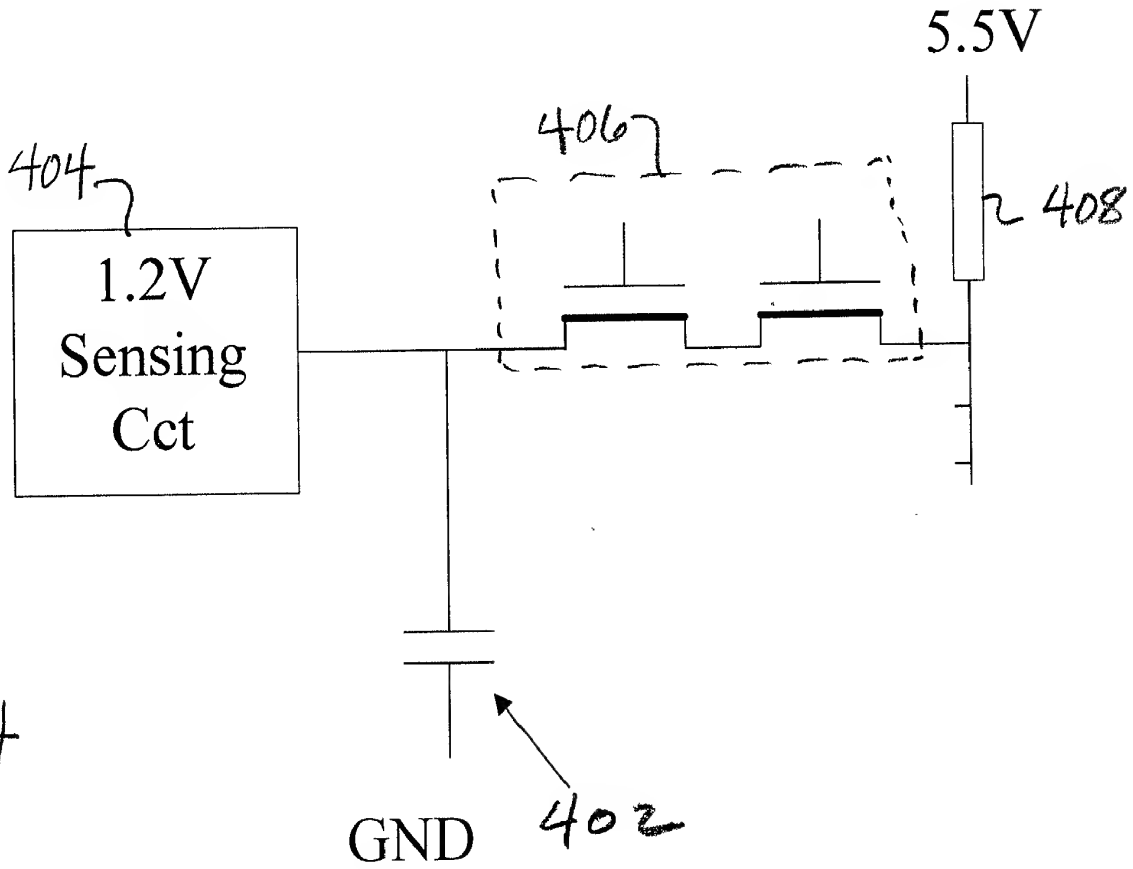

FIG. 4

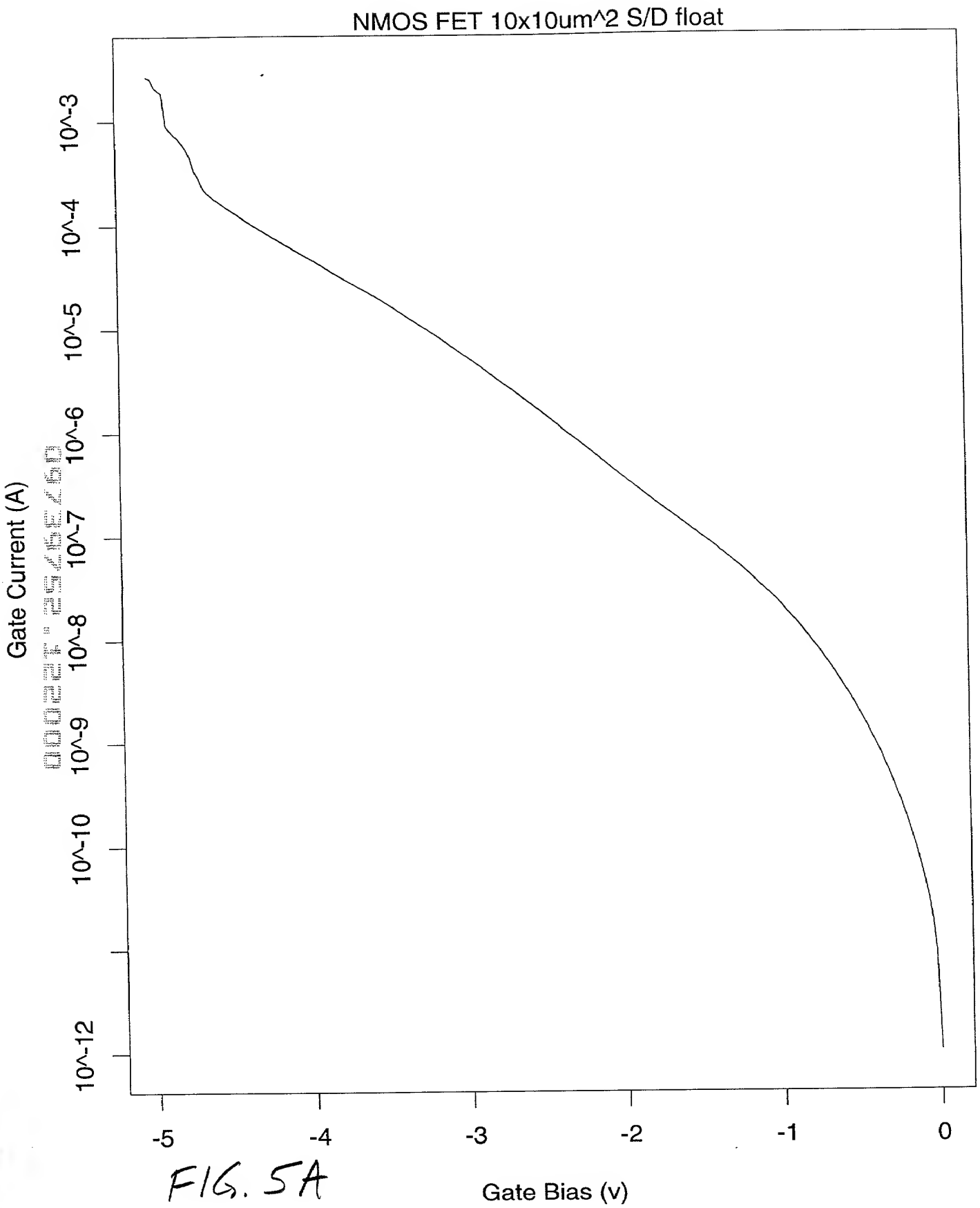
NMOS FET 10x10um^2 S/D float
Gate Current (A)
10^-3
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-12
-5
-4
-3
-2
-1
0
Gate Bias (v)

FIG. 5A

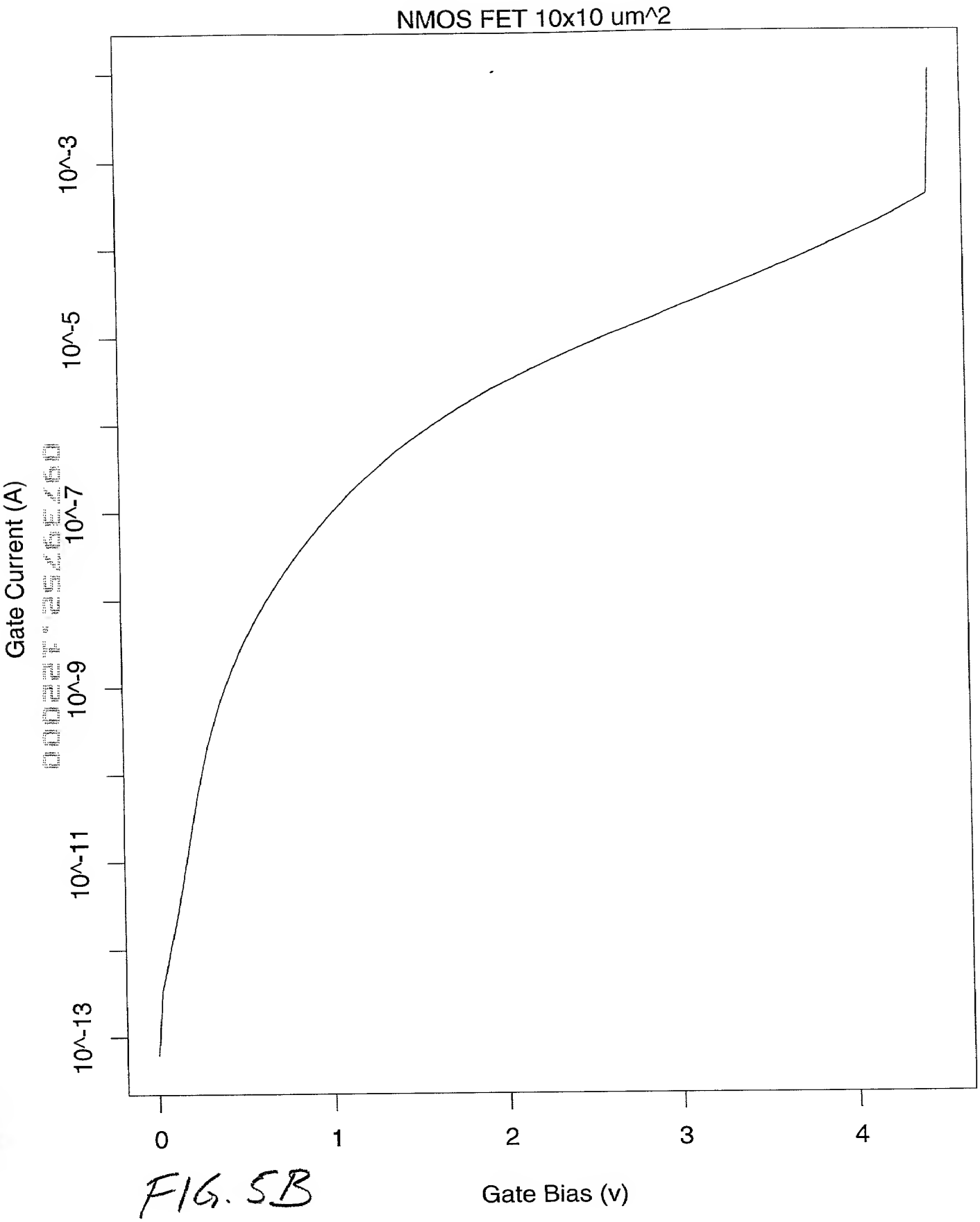
NMOS FET 10x10 um^2
Gate Current (A)
10^-3
10^-5
10^-7
10^-9
10^-11
10^-13
0
1
2
3
4
Gate Bias (v)

FIG. 5B

GATE OXIDE FUSE

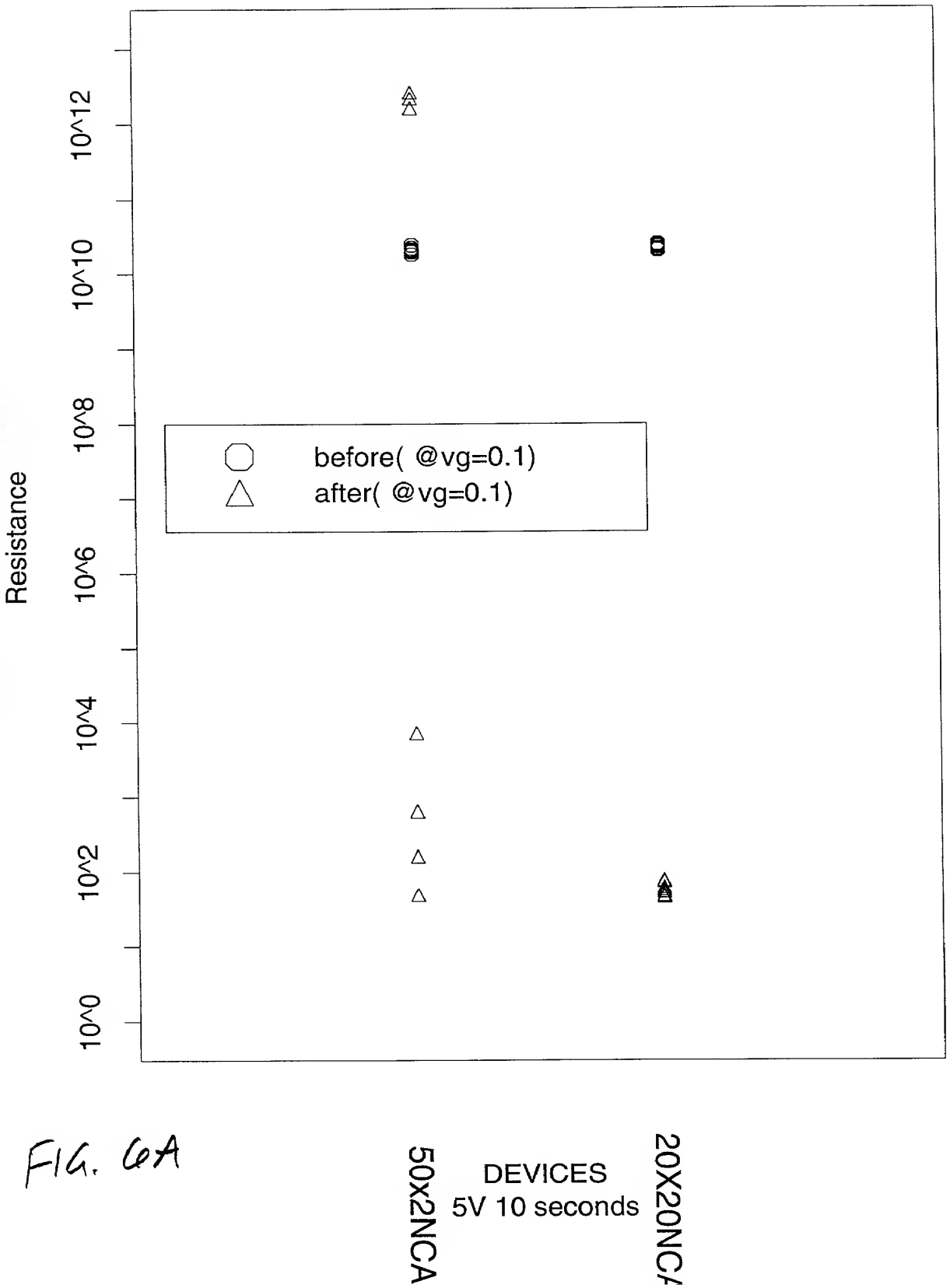

FIG. 6A

GATE OXIDE FUSE

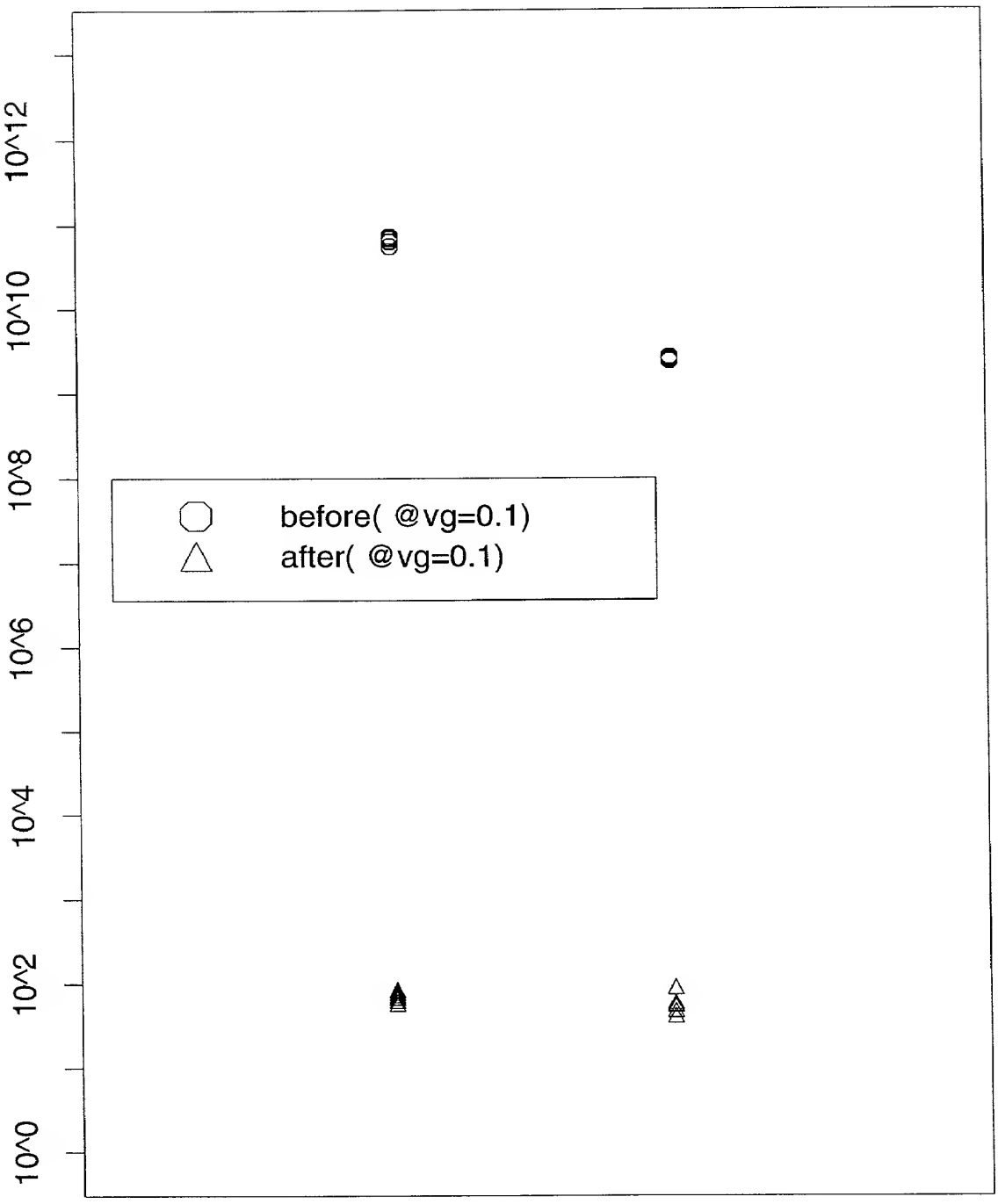

FIG. 6B

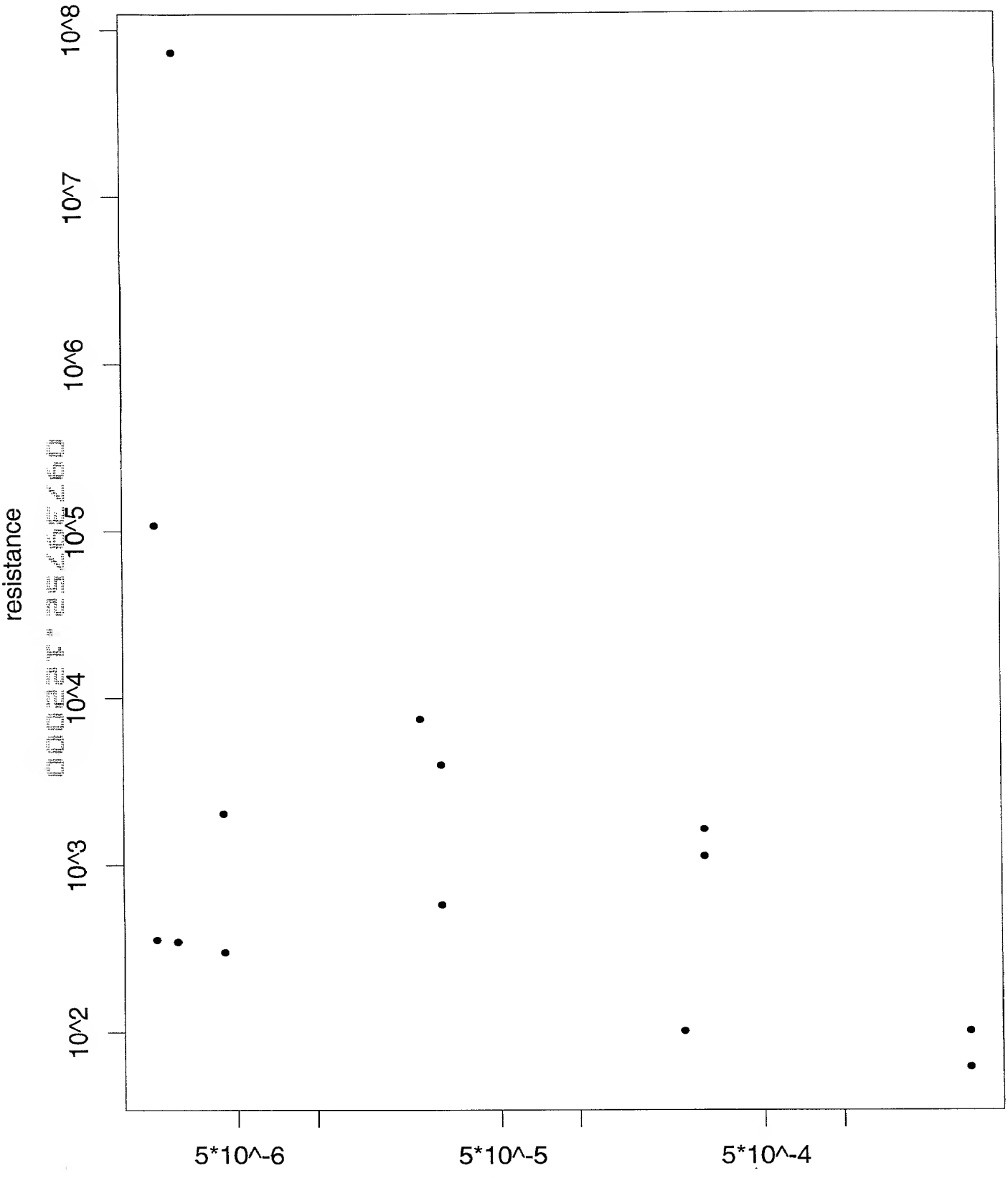
resistance
10^8
10^7
10^6
10^5
10^4
10^3
10^2
5*10^-6
5*10^-5
5*10^-4
Max Power(FuseV*I_comp*FuseT)

FIG. 7